formed can be larger than a width (W2) thereof in portions in which the contact holes **110** are not formed (W1>W2).

[0087] By adopting such a configuration, in addition to the effects obtained in Embodiments 1 and 2 mentioned above, it becomes possible to lengthen a length (channel width of the transistors) of peripheries of the trenches **105** while keeping a distance (L1) between the trenches and the contact holes at a value predetermined by specifications and the like. In such a way, it becomes possible to reduce the ON-resistance of the MOSFET, and the low-loss semiconductor device can be provided. Here the distance (L1) between the trenches and the contact holes is a distance between the side surfaces of the trenches and the side surfaces of the contact holes **110**.

[0088] In a configuration shown in FIG. **6**, with respect to the configuration shown in FIG. **5**, the contact holes **110** formed in the individual trenches **105** adjacent to one another are arranged alternately (so as not to be opposite to one another). Others are similar to those of the configuration of FIG. **5**.

[0089] By adopting such a configuration, in comparison with the configuration shown in FIG. **5**, it becomes possible to shorten a gate pitch (L3) in comparison with that of the configuration shown in FIG. **5** shown above while maintaining an inter-gate electrode distance (L2) similarly to that of the configuration shown in FIG. **5**. In such a way, in comparison with the configuration shown in FIG. **5**, the integration degree of the semiconductor device can be further enhanced. Moreover, it becomes possible to reduce the ON-resistance of the MOSFET, and the low-loss semiconductor device can be provided. Here, as shown in FIG. **5** and FIG. **6**, the inter-gate electrode distance (L2) is a distance between the gate electrodes **108** formed in the trenches **105** adjacent to one another, and the gate pitch (L3) is a distance between centers of the trenches **105** adjacent to one another.

[0090] In a configuration shown in FIG. **7**, the trenches **105** are formed into a mesh shape. In this mesh, each section thereof has a quadrangular shape as shown in FIG. **7**. The contact holes **110** are arranged on individual intersections of the mesh (that is, on portions at which the longitudinal and lateral trenches **105** intersect one another).

[0091] By adopting such a configuration, it becomes possible to enhance a density of the mesh while keeping the distance (L1) between the trenches and the contact holes at the value predetermined by the specifications and the like. In such a way, the integration degree of the semiconductor device can be enhanced. Moreover, it becomes possible to reduce the ON-resistance of the MOSFET, and the low-loss semiconductor device can be formed with good controllability.

[0092] In a configuration shown in FIG. **8**, the trenches **105** are formed into a mesh shape in a similar way to the case in FIG. **7** shown above; however, the configuration shown in FIG. **8** is different from that shown in FIG. **7** in that each section of the mesh has a hexagonal shape. The contact holes **110** are arranged on individual vertices of the mesh (that is, on portions at which the trenches **105** intersect one another).

[0093] By adopting such a configuration, it becomes possible to enhance the density of the mesh while keeping the distance (L1) between the trenches and the contact holes at the value predetermined by the specifications and the like. In such a way, the integration degree of the semiconductor device can be enhanced. Moreover, it becomes possible to reduce the ON-resistance of the MOSFET, and the low-loss semiconductor device can be formed with good controllability.

[0094] Note that, though the above description illustrates the case where the shape of each section of the mesh is the quadrangular shape and the hexagonal shape, the shape of the section may be other polygonal shapes or circular. In that case, the contact holes **110** can be arranged on vertices of a polygon or along a circumference of a circle.

Embodiment 4

[0095] FIG. **9** to FIG. **11** are plan views showing layouts in a plane direction (main surface direction of a semiconductor substrate) of a semiconductor device according to Embodiment 4 of the present invention.

[0096] FIG. **9** to FIG. **11** are views when states where the source electrode **112** of the semiconductor device shown in FIG. **1** is removed are viewed. While the contact holes **110** are arranged discretely in FIG. **5** to FIG. **8**, which are shown above, the contact holes **110** are formed continuously in each of layout examples shown in FIG. **9** to FIG. **11**.

[0097] In a configuration shown in FIG. **9**, the contact holes **110** are formed on straight lines along the insides of the trenches **105** formed in a longitudinal direction of a sheet surface.

[0098] By adopting such a configuration, the contact holes **110** are formed continuously, and accordingly, it becomes possible for the anode regions **106** to connect to the source electrodes **112** continuously embedded in the contact holes **110** immediately above the same. In such a way, a contact area between the anode regions **106** and the source electrodes **112** is increased, and both thereof can be connected to each other at a low resistance. As a result, such a low-loss semiconductor device in which the ON-resistance of the diode is reduced can be provided.

[0099] In a configuration shown in FIG. **10**, the trenches **105** are formed into a mesh shape in which each section is quadrangular in a similar way to the case shown in FIG. **7** shown above, and the contact holes **110**, and the contact holes **110** are also formed continuously into a mesh shape along the insides of the trenches **105** with the mesh shape.

[0100] In a configuration shown in FIG. **11**, the trenches **105** are formed into a mesh shape in which each section is hexagonal in a similar way to the case shown in FIG. **8** shown above, and the contact holes **110** are also formed continuously into a mesh shape along the insides of the trenches **105** with the mesh shape.

[0101] By adopting such configurations, the contact holes **110** are formed continuously, and accordingly, it becomes possible for the anode regions **106** to connect to the source electrodes **112** continuously embedded in the contact holes **110** immediately above the same. In such a way, the contact area between the anode regions **106** and the source electrodes **112** is increased, and both thereof can be connected to each other at a low resistance. As a result, the low-loss semiconductor device in which the ON-resistance of the diode is reduced can be provided.

[0102] As above, in the respective Embodiments 1 to 4 mentioned above, while a unit cell is illustrated in each cross-sectional view of the semiconductor devices, a parallel connection structure in which a plurality of the unit cells is aggregated and repeated may be formed. Moreover, an electric field relaxation structure composed of a guard ring or a